changing an instruction set architecture under which instructions are interpreted by the computer in the handler software for the interrupt.

33. (new) The method of claim 32, wherein the instruction text beginning at the returned-to instruction is logically equivalent to the instruction text beginning at the interrupted instruction.

34. (new) The microprocessor chip of claim 30, further comprising:

table lookup circuitry designed to index into a table by a memory address of a memory reference arising during execution of an instruction, and to retrieve a table entry corresponding to the address;

the instruction pipeline circuitry being responsive to the contents of the table to affect a manipulation of data or transfer of control defined for the instruction.

REMARKS

Applicant respectfully requests reconsideration of the application. Claims 1-34 are now pending. Claims 1, 2, 10, 14, 19, 24 and 30 are independent.

Applicant thanks the Examiner for the productive interview of September 25, 2000. This was a purely informational interview – Applicant did not request any reconsideration of any issues of patentability, and no resolutions were reached. The general idea behind the invention was discussed, and the Examiner presented his view on the scope of several claims. Though such interchange, understanding was improved for both Applicant and Examiner.

Most of the amendments to the specification are directed to conforming the specification to itself, to resolve inconsistencies in the naming of certain elements. The text added at page 89, line 31, is supported by Table 1 (page 34 of the specification) and Fig. 5a. Because this new text merely explains what was already present in the Table and Figure, this amendment introduces no new matter.

Formal drawings are provided. These drawings make minor corrections to the informal drawings originally filed, for instance to correct the inconsistency in the use of certain reference numbers noted by the Examiner.

The amendments to the claims address the rejections under § 112 ¶ 2, and are not made for a substantial reason related to patentability.

Section 112 ¶ 2 rejections

Several rejections are raised under § 112 ¶ 2. Many of these rejections are addressed by the amendments to the claims.

The § 112 ¶ 2 rejection queries:

> The claims fail to recite function of the address translation circuitry. It is not clear what type of address it is translated from and into.

"Address translation" is a well-known term of art, as demonstrated by the appearance of the term in several processor architecture guides and undergraduate textbooks (see accompanying Exhibit). Because the term is well-understood in the art, and the term is used in the claims in the art's conventional sense, Applicant respectfully suggests that the term is not indefinite. (As discussed below, there is no requirement under § 112 ¶ 2 that a claim recite the "function" of an element – "function" is an entirely optional form of claiming, for instance under § 112 ¶ 6 or MPEP § 2173.05(g), not a mandatory form under § 112 ¶ 2.)

The rejection continues:

> In claim 4, the ISA 184 shown in Figure 1a is described in line 20 of page 39 as write-protect bit and not instruction set architecture as recited in claim 4. Applicant is requested to review the entire specification and drawings for any possible errors. Applicant is cautioned not to introduce any new matter.

This rejection is addressed by the amendments to the drawings.

The Examiner requests clarification of the following:

> 1. "to effect control of an architecture-visible data manipulation behavior of control transfer behavior of the instruction." It is not clear what actually the instruction does.

Some instructions have a "data manipulation behavior" – for instance, an ADD instruction calls for an addition ("data manipulation" behavior can be contrasted to "data movement" behavior of a memory load or store). An instruction may have a "control transfer behavior" – for instance, a JUMP instruction calls for a control transfer to a particular program location. One example of "controlling the behavior" would be observed if two instructions that have identical instruction bits did two behaviorally-different things, with the difference based on the "controlling." In one case, the same bit pattern might be an ADD based on one way of controlling the behavior, and a JUMP based on another. A "control transfer behavior" would be affected if the architectural definition of a JUMP called for a transfer to one location, and the instruction actually executed as a transfer to an entirely different location. Because the claim language would be well-

understood by one of ordinary skill in the art, and (to Applicant's knowledge) has no better-known synonym in the art, Applicant respectfully requests that the indefiniteness rejection be withdrawn.

The Examiner queries the meaning of the following:

> 2. "the architectural definition of the instruction not calling for an interrupt" in line 14 of claim 1.

An "instruction whose architectural definition does not call for an interrupt" is an instruction that the architecture defines as executing without raising an interrupt. For instance, in most computers, the definition of an integer add of two integer registers, where one register contains "2" and the other contains "3," does not call for an interrupt. On the other hand, as is well-known in the art, the definition of an SVC instruction calls for an interrupt. Because the claim language is conventional idiomatic usage within the art, Applicant respectfully requests that the indefiniteness rejection be withdrawn.

The rejection queries the meaning of the following:

> 2. "execution control" in line 2 of claim 3. What is being executed or controlled and the execution cotrol [sic] of which is being transferred to a different instruction for execution? It appears that execution control of an instruction can not be transferred to a different instruction for execution.

The question demonstrates that claim 3 is understood. In one possibility, claim 3 reads on an implementation in which "execution control of an instruction [is] transferred to a different instruction for execution." A claim with a scope that is clearly understood is not "vague and indefinite."

In several of these cases, the claims are directed to features that are not encountered in the art frequently enough to have well-established names. Applicant has had to coin new terms. If the Examiner is aware of a well-known synonym for any of the concepts described here, Applicant will be happy to adopt any reasonable suggestion.

Applicant respectfully requests that the Examiner reconsider the remaining rejections under § 112 ¶ 2 to evaluate whether these rejections are properly grounded in reasoning authorized in the MPEP. The following rejections are traversed:

> Claims 1-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
>
> There is no functional relationship between the address translation circuitry and the other components. The pipeline, the table lookup circuit, and the interrupt circuit or the handler have no use of the translated addresses.

> It is not seen how the likelihood of the existence of an alternate coding of instruction (line 6, claim 1 for example) would cause the handler to affect the instruction pipeline circuitry to effect control of an architecturally-visible data manipulation behavior or control transfer behavior of the instruction (line 15 of claim 1 for example). It appears that there is no relationship between them.
>
> ...
>
> With respect to all the claims, it is not seen why the interrupt to effect control of behavior of an instruction is triggered by memory state and instruction address.

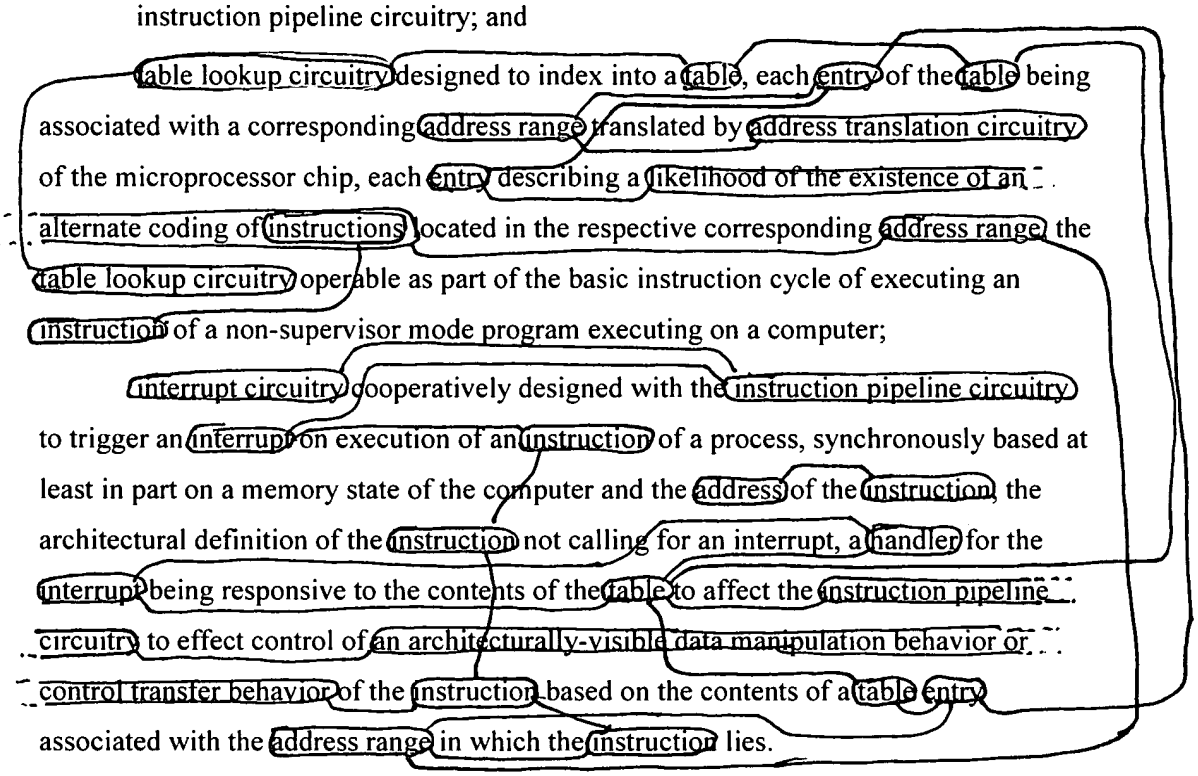
In the same vein, during the interview of September 25, 2000, the Examiner queried whether the invention was "useful as claimed."

It appears that these rejections confuse the utility requirement of § 101, the enablement requirement of § 112 ¶ 1, and the "distinctly claim" requirement of § 112 ¶ 2. For instance, the question of whether an invention is "useful as claimed" is relevant under § 101, but is irrelevant under § 112 ¶ 2. Questions about why something happens, functional relationships, uses of intermediate results, or how one element "affects" another may be relevant under the "how to make" and "how to use" requirements under § 112 ¶ 1, but are irrelevant under § 112 ¶ 2. Questions arising under § 101 or § 112 ¶ 1 may be answered by reference to the specification; there is no requirement under § 112 ¶ 2 that the claims set out such relationships, uses, causes, effects, or functions to be definite.

The Interview Summary points to MPEP §§ 706.03(d) and 2172.01 as the basis for "incompleteness" as a ground of rejection. These two sections confirm that "incompleteness" is not invoked by the types of concerns queried in the rejection. Rather, "incompleteness" is only a proper ground of rejection when either (i) some statement by applicant states that an element is "essential," or (ii) where a claim has a gap, a complete disconnection from, between one element or group of elements and another. For instance, here is the most relevant form paragraph from MPEP § 706.03(d) (underline added):

> ¶ 7.34.13 *Essential Elements Omitted*
>
> Claim [1] rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: [2]
>
> Examiner Note:
>
> 1. This rejection must be preceded by form paragraph 7.30.02 or 7.103.
>
> 2. In bracket 2, recite the elements omitted from the claims
>
> 3. Give the rationale for considering the omitted elements critical or essential.

Here is claim 1, showing the interrelationships between claim elements. Red links join mentions of the same element, green links show interrelationships among elements. As can be seen, between every pair of elements, there is at least one chain of interrelationship:



1. A microprocessor chip, comprising:

instruction pipeline circuitry; and

table lookup circuitry designed to index into a table, each entry of the table being associated with a corresponding address range translated by address translation circuitry of the microprocessor chip, each entry describing a likelihood of the existence of an alternate coding of instructions located in the respective corresponding address range, the table lookup circuitry operable as part of the basic instruction cycle of executing an instruction of a non-supervisor mode program executing on a computer;

interrupt circuitry cooperatively designed with the instruction pipeline circuitry to trigger an interrupt on execution of an instruction of a process, synchronously based at least in part on a memory state of the computer and the address of the instruction, the architectural definition of the instruction not calling for an interrupt, a handler for the interrupt being responsive to the contents of the table to affect the instruction pipeline circuitry to effect control of an architecturally-visible data manipulation behavior or control transfer behavior of the instruction based on the contents of a table entry associated with the address range in which the instruction lies.

It is seen that every element is, at least indirectly, connected to every other. In particular, the "address translation circuitry" is interconnected to the entries of the table at lines 3-4, and from there to the rest of the elements of the claim. Because there is no "omission amounting to a gap between the elements," no rejection can be based in MPEP § 706.03(d).

MPEP §§ 706.03(d) and form paragraphs 7.34.12-14 refer to MPEP § 2172.01 for the definition of "incompleteness." MPEP § 2172.01 only authorizes an "incompleteness" rejection when the applicant has defined some element as "essential" or "necessary" (citations omitted):

> **2172.01 Unclaimed Essential Matter**
>
> A claim which omits matter disclosed to be essential to the invention as described in the specification or in other statements of record may be rejected under 35 U.S.C. 112, first paragraph, as not enabling. Such essential matter may include missing elements, steps or necessary structural cooperative relationships of elements described by the applicant(s) as necessary to practice the invention.
>
> In addition, a claim which fails to interrelate essential elements of the invention as defined by applicant(s) in the specification may be rejected under 35 U.S.C. 112, second paragraph, for failure to point out and distinctly claim the invention.

It is believed that none of the elements of claim 1 are described as being either "essential" or "necessary" in the specification or in any other statement by Applicant. Thus, neither prong of MPEP § 2172.01 can be satisfied, and no "incompleteness" rejection can lie.

The observation that "The pipeline, the table lookup circuitry and the interrupt circuit or the handler have no use of the translated address" is not addressed to any ground of rejection under § 112 ¶ 2. A claim need not explicitly recite all $(n^2-n)/2$ interrelationships among n elements – indirect interconnections (as shown above) are sufficient. For instance, in the Adachi '975 patent, there is no recited interrelationship between the "operand value" of claim 1 and the "operation system of said target machine." Yet, because Adachi's claim relates both to the "interrupt instruction," the claim is definite. Similarly, because all elements of claim 1 of this application are directly or indirectly interconnected, claim 1 is definite.

Every claim *must end somewhere*, with a final step or element that "has no use" recited in the claim. Any such rule requiring a "use" of every element would be unenforceable: adding a new element to provide a "use" for an existing element would just beg the next question – where is the "use" for that new element?

Because the rejection does not arise under any proper ground, it may be withdrawn.

If any concern remains under any one of § 101, § 112 ¶ 1 or § 112 ¶ 2, Applicant requests a rejection that properly analyzes the application under the relevant *prima facie* test. However, the MPEP does not authorize a "mix and match" approach in which a rejection may be supported by some reasoning from one statutory section and other reasoning from another section.

One episode of the interview of September 25 illustrates many of the issues underlying the remaining rejections under § 112 ¶ 2. The Examiner expressed the opinion that claim 14 was vague and indefinite, and appeared to be mis-drafted – and then, with no prompting or explanation from Applicant, volunteered a paraphrase of the claim that demonstrated clear understanding of the claim. A readily-understood claim is rarely "vague and indefinite."

Applicant would welcome a telephone call to clarify any future questions relating to the subject matter being claimed. Applicant's experience is that prosecution advances much more efficiently when questions are asked by phone rather than by rejection.

Rejection under § 103(a) of claim 2

Claim 2 recites that "the table [is] addressed by the address of instructions executed." This limitation is nowhere mentioned in the Office Action. Because the rejection is incomplete, Applicant respectfully observes that no *prima facie* case of obviousness has been raised.

Further, as is well known in the art, the SVC instruction of Adachi '975 patent does not use such a table. Rather, Adachi's SVC instruction has an immediate field (Adachi '975, col. 4, lines 55-56) embedded in the instruction, and Adachi's SVC jump table is indexed by the value of that immediate (col. 4 lines 52-55). The contents of an instruction (as in Adachi) are quite different than the address of the instruction (as recited in the claim). Adachi '975 refers to "address" several times in col. 4, but this is the address of the SVC jump table, not of the SVC instruction itself (*e.g.*, every SVC will refer to the SVC jump table at the same address, independent of the address of the SVC itself). Because the claim recites an element entirely absent from the prior art, no *prima facie* obviousness rejection can be raised. MPEP § 2143.03.

Rejection under § 103(a) of claim 10

Claim 10 recites as follows:

> 10. A microprocessor chip, comprising:
>
> instruction pipeline circuitry;
>
> table lookup circuitry designed to index into a table by a memory address of a memory reference arising during execution of an instruction, and to retrieve a table entry corresponding to the address, the table entry being distinct from the memory referenced by the memory reference;
>
> the instruction pipeline circuitry being responsive to the contents of the table to alter a manipulation of data or transfer of control behavior of the instruction in a manner incompatible with the architectural definition of the instruction.

As is well known in the art, an SVC instruction is defined to execute as follows: (a) fetch an address of an SVC jump table, (b) fetch a value from the SVC jump table based on the value of an immediate value coded into the SVC instruction, and (c) transfer control to the address fetched from the SVC jump table. Nothing in Adachi's disclosure suggests that the behavior of Adachi's SVC instruction departs from the conventional architectural definition of an SVC instruction. Adachi manages the contents of his SVC jump table to achieve a specific result, but does nothing to alter he behavior of the SVC instruction itself in a manner inconsistent with its architectural definition.

In contrast, claim 10 recites an instruction whose execution is altered in a manner incompatible with its architectural definition.

Because the claim recites an element entirely absent from the prior art, no *prima facie* obviousness rejection can be raised. MPEP § 2143.03. Because the rejection is incomplete, Applicant respectfully observes that no *prima facie* case of obviousness has been raised.

The rejection of claim 1 is incomplete for similar reasons, and may be withdrawn.

Rejection of claim 14 under § 103(a)

Claim 14 recites as follows:

> 14. A microprocessor chip, comprising:
>
> instruction pipeline circuitry;
>
> address translation circuitry; and
>
> a lookup structure having an entry associated with each corresponding address range translated by the address translation circuitry, the entry describing a likelihood of the existence of an alternate coding of instructions located in the respective corresponding address range.

The limitation "the entry describing a likelihood of the existence of an alternate coding of instructions located in the respective corresponding address range" is nowhere discussed in the rejection under § 103(a). Because the rejection is incomplete, Applicant respectfully observes that no *prima facie* case of obviousness has been raised.

The rejection of claim 1 is incomplete for similar reasons, and may be withdrawn.

Rejection of claim 19 under § 103(a)

Claim 19 reads as follows:

> 19. A microprocessor chip, comprising:
>
> instruction pipeline circuitry; and
>
> interrupt circuitry cooperatively designed with the instruction pipeline circuitry to trigger an interrupt on execution of an instruction of a process, synchronously based at least in part on a memory state of the computer and the address of the instruction, the architectural definition of the instruction not calling for an interrupt.

The limitation "trigger[ing] an interrupt on execution of an instruction..., the architectural definition of the instruction not calling for an interrupt" is mentioned in the rejection under § 112 ¶ 2, but is nowhere discussed in the rejection under § 103(a). MPEP § 2143.03 instructs that all claim limitations must be addressed in a rejection under § 103(a); even "a claim limitation which

is considered indefinite cannot be disregarded." Because the rejection is incomplete, Applicant respectfully observes that no *prima facie* case of obviousness has been raised.

The rejection of claim 1 is incomplete for similar reasons, and may be withdrawn.

Observation and request

MPEP §§ 2143-2143.03 sets out a three-step test for analyzing the "obviousness of the difference" between a claim and the prior art, and states that this is the test that "must" be used. Applicant requests that any future rejections under § 103(a) make the three showings required by MPEP § 2143.

Dependent claims

The Office Action purports to reject all of the dependent claims under § 103(a). However, most of these claims recite limitations that are not addressed anywhere in the § 103(a) portion of the Action. Such piecemeal examination is discouraged by 37 C.F.R. § 1.105 and MPEP § 707.07(g). It is requested that any future Office Action indicate the allowability of any claim that recites a limitation against which no prior art is cited.

Conclusion

In view of the amendments and remarks, Applicant respectfully submits that the claims are in condition for allowance. Applicant requests that the application be passed to issue in due course. The Examiner is urged to telephone Applicant's undersigned counsel at the number noted below if it will advance the prosecution of this application, or with any suggestion to resolve any condition that would impede allowance. In the event that an extension of time is required, Applicant petitions for that extension of time required to make this response timely.

Kindly charge any additional fee, or credit any surplus, to Deposit Account 50-0324, Order No. 30585/16.

Respectfully submitted,

SHEARMAN & STERLING

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